A New Hardware Structure for Implementation of Soft Morphological Filters

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Abstract : A new hardware structure for implementation of soft morphological filters is presented in this paper. This is based on the modification of the majority gate technique. A pipelined systolic array architecture suitable to perform real-time soft morphological filtering is presented as an illustrative example. The processing times of the proposed hardware structure do not depend on the data window size and its hardware complexity grows linearly with the number of its inputs.

1 Introduction

Mathematical morphology is a methodology for image analysis and image processing, based on set theory and topology [1]. It offers effective solutions to many computer vision problems including noise removal, feature extraction, texture analysis, skeletonizing etc. Dilation and erosion are the two basic morphological operations. In mathematical morphology primary role has the structuring element (s.e.). Many morphological filters, based on the two basic operations, have been have been studied [2]. Another well studied class of non-linear filters are rank order filters, which have excellent robustness properties and have been applied into many image processing applications [3]. Soft morphological filters are a combination of morphological and rank order filters [4]. They have been introduced to improve the behaviour of traditional morphological filters in noisy environments. They are less sensitive to additive noise and to small variations in object shape than the standard morphological filters.

Soft morphological filters is a relatively new class of non-linear filters, and therefore, only a few designing methods have been reported [4]. Soft morphological filters can be VLSI implemented using the threshold decomposition technique [5]. However, in this approach hardware complexity increases exponentially both with the resolution of the numbers and the size of the data window. Therefore, implementation of filters capable of handling high resolution numbers is not practical. In this paper a pipelined systolic array is presented, capable of implementing soft morphological dilation (s.m.d.) and soft morphological erosion (s.m.e.). This hardware structure is based on the majority gate technique [6]. This technique has been applied for both morphological filtering [7] and rank order filtering [8] and, thus, it is suitable for their combination, i.e. soft morphological filtering. The architecture of the proposed hardware structure is scalable; its hardware complexity grows linearly with the number of inputs and its processing times do not depend on the data window size.

2 Soft Morphological Operations

In soft morphological operations the max/min operations, used in standard morphology, are replaced by weighted order statistics and the s.e. B is divided into two subsets, i.e. the core A and the soft boundary B\A ("\" denotes the set difference). In s.m.d. (s.m.e.) the pixels of the image are combined with the pixels of the s.e. as in standard morphology; the results which are related to the soft boundary of the s.e. and the results which are related to the core of the s.e. are repeated k times and ordered in a descending (ascending) sequence. The kth element of this sequence is the result of s.m.d. (s.m.e.). Let $\{k \Diamond f(x)\}$ denote the k time repetition of $f(x)$; $\{k \Diamond f(x)\} = \{f(x), f(x), \ldots f(x)\}$ (k times). The s.m.d. of a gray-scale image f by a soft gray-scale s.e. $[\alpha, \beta, k]$ is defined as [4] :

$$f \oplus [\beta, \alpha, k](z) = k\text{th larger of } \left(\left\{k\Diamond\left(f(y) + \alpha(z-y)\right)\right\} \cup \left\{f(b) + \beta(z-b)\right\}\right) \quad (1)$$

where $(z-y) \in \mathrm{A}$ and $(z-b) \in \mathrm{B} \setminus \mathrm{A}$.

Also the s.m.e. of f by $[\alpha, \beta, k]$ is defined as :

$$f \ominus [\beta, \alpha, k](z) = k\text{th smaller of } \left(\left\{k\Diamond\left(f(y) - \alpha(z+y)\right)\right\} \cup \left\{f(b) - \beta(z+b)\right\}\right) \quad (2)$$

where $(z+y) \in \mathrm{A}$ and $(z+b) \in \mathrm{B} \setminus \mathrm{A}$.

Based on the above definitions (eqns (1) and (2)) a hardware structure that computes s.m.d/s.m.e. can be constructed. This consists of adders/subtractors, followed by a module, which computes the required order statistic of the addition/subtraction results. The aforementioned module is implemented using the algorithm, which was first presented in [8] and it is suitable for rank order filtering. This algorithm applies a median computation algorithm [6] to a sequence of numbers and uses additional dummy inputs. By computing the median value of the expanded sequence and by being able to control the dummy numbers, any order statistic of the original sequence of the numbers can be determined. Figures 1a, 1b and 1c illustrate this concept. The dummy numbers are used for the computation of median, 2nd order statistic and maximum values, respectively. The bold window contains five binary numbers $x_{(1)}$, $x_{(2)}$, ...$x_{(5)}$ in an ascending order (the subscript in the parentheses denotes the rank). The larger window contains nine binary numbers also in an ascending order. By controlling the dummy numbers d_i which are pushed to the top and to the bottom, any order statistic r of the numbers x_i, can be obtained.

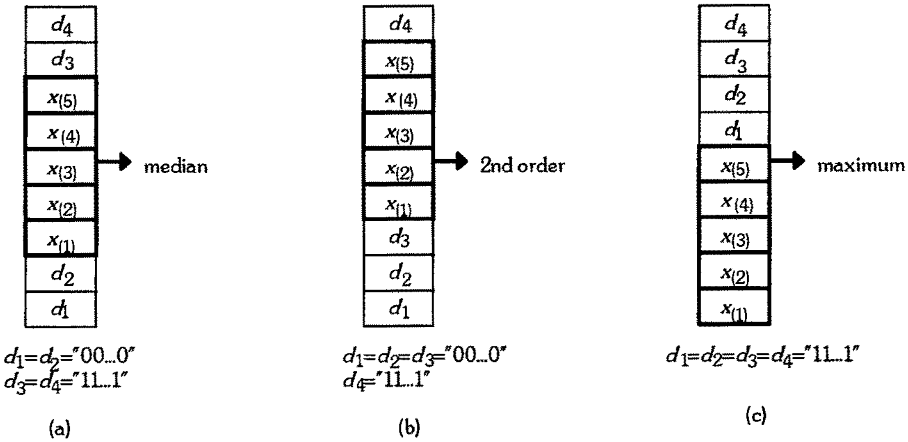

Fig. 1. Illustration of dummy inputs use : (a) median, (b) 2nd order and (c) maximum computation.

3 Systolic Array Implementation for Soft Morphological Filtering

A pipelined systolic array (Figure 2) capable of computing s.m.d./s.m.e. using a four neighbor s.e. and eight bit resolution images is presented in this section. The inputs to this array are five pixels of the image window, five pixels of soft morphological s.e. (this includes the core, the soft boundary and k) and a control signal MODE. The central pixel of the s.e. is its core, whereas the rest four neighbor pixels are the soft boundary. The first five latches (L1) hold the image window, the next five latches (L*1) hold the s.e. and the remaining one (L**1) holds number k. Global signal MODE is used to select the operation; "1" selects the s.m.d., whereas "0" selects the s.m.e. operation. It can be seen from eqns (1) and (2) that in s.m.d. the reflection of the s.e., with respect to the origin, interacts with the image window, whereas in s.m.e. it interacts exactly with the image pixels it overlays. Image data is collected by five multiplexers MUX1, which are controlled by the signal MODE. In the same stage the pixels of s.e. remain either unchanged when the operation of s.m.d. is considered or they are complemented in the operation of s.m.e., by means of XNOR gates controlled by the signal MODE. In the next stage of the pipeline, data is fed to five adders. In the case of s.m.e. the 1's complements of the pixels of the s.e. are added to the image data and the carry in (C_{in}) bit to the adder is "1". Thus, the 2's complements of the pixels of the s.e. are added to the image pixels. This is equivalent to the subtraction operation.

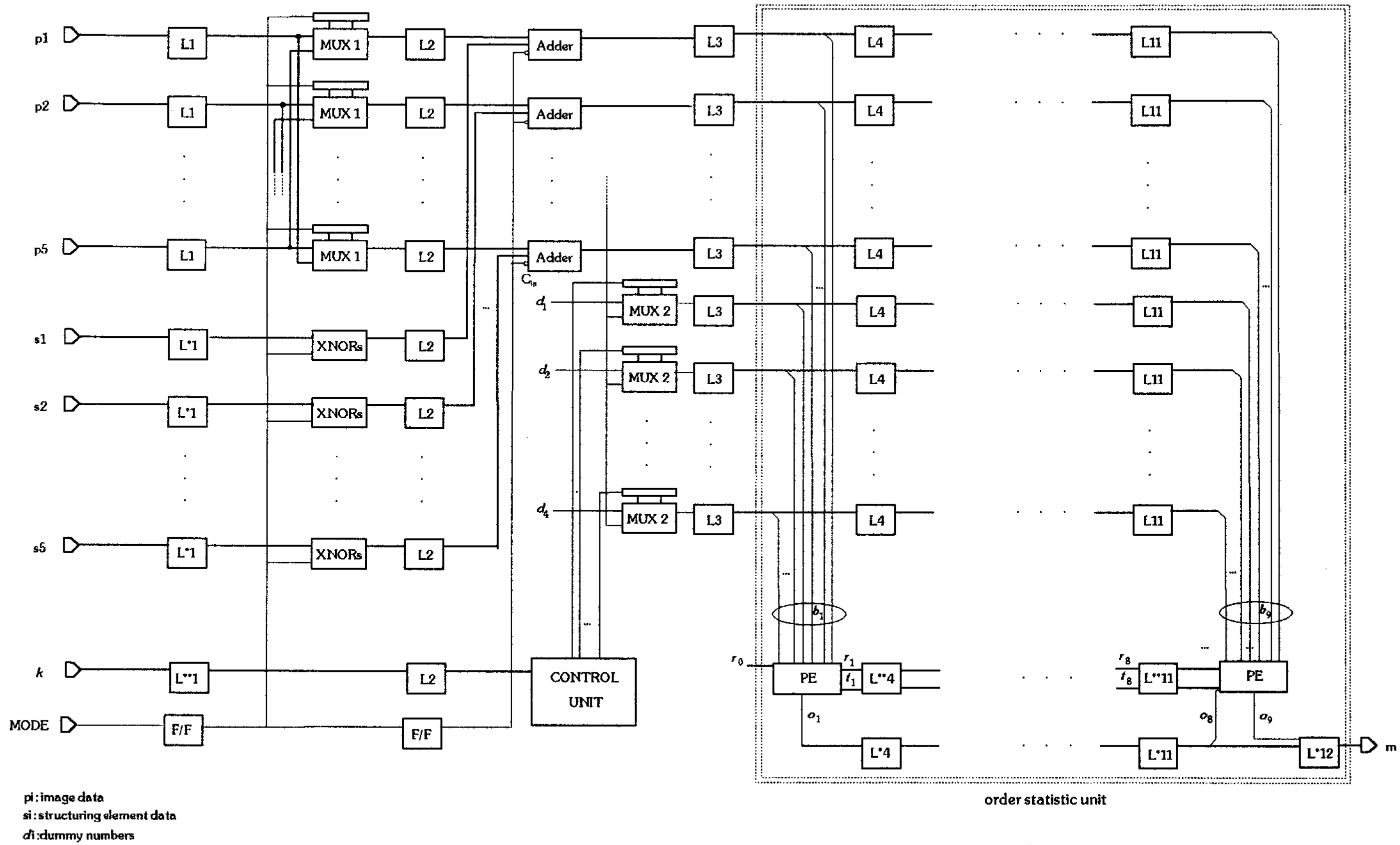

Fig. 2. Systolic array hardware structure implementing the majority gate technique for soft morphological filtering.

In soft morphological filtering, if k > Card(B\A), then the soft morphological operations are reduced and only the core of the s.e. is considered [5]. Therefore in order to preserve the nature of soft morphological operations, the constraint that $k \leq \min\{Card(B)/2, Card(B/A)\}$ is used. In this case : Card(B)=5, Card(A)=1, Card(B\A)=4 and $k \leq \min\{2.5, 4\} \Rightarrow 1 \leq k \leq 2$. Figure 3a illustrates the position of the dummy numbers in s.m.d. for k =1 and k=2, whereas Figure 3b illustrates the position of the dummy numbers in s.m.e. For s.m.d. all the dummy inputs are pushed to the top, whereas for s.m.e. they are pushed to the bottom. Thus, the appropriate result is obtained from the order statistic unit. A control unit, the input of which is the number k, controls an array of multiplexers MUX2 and inputs to the order statistic unit either a dummy number or a copy of the addition/subtraction result of the core. The order statistic unit consists of identical Processing Elements (PEs) separated by latches (L**4 to L**11). The block diagram of the PE is shown in Figure 4. In each PE the bits ($b_{1,j}...b_{9,j}$) of the same significance of the numbers of the resulting sequence are processed, starting with the most significant bits in the first stage until the less significant bits in the last stage. The process is based on the majority selection of intermediate signals ($i_{1,j}...i_{9,j}$). The selection is achieved using a majority gate, which operates as follows : its output (o_{j+1}) is "1", if over half of its inputs are "1"; otherwise its output is "0". Flag signals ($r_{1,j}...r_{9,j}, t_{1,j}...t_{9,j}$) derived from previous stages are used for further processing in the successive stages, in order to show whether a number has been rejected or not. At the end of the process the median value of the resulting sequence is obtained, which, by appropriate choice of the dummy numbers through the control unit, is the result of the soft morphological operation.

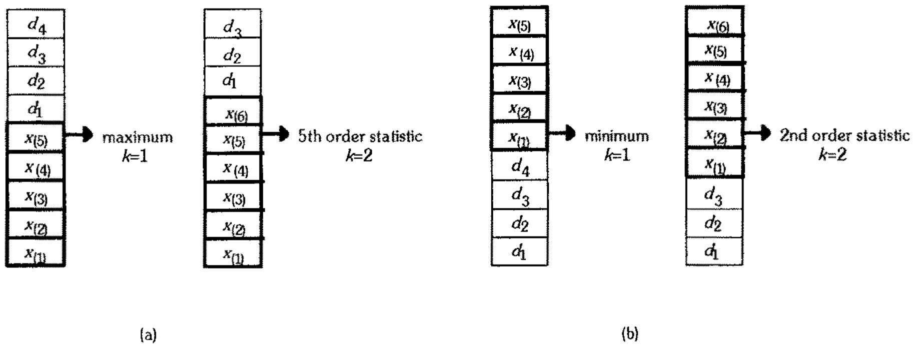

Fig. 3. (a) Arrangement of the dummy numbers for s.m.d. and (b) arrangement of the dummy numbers for s.m.e.

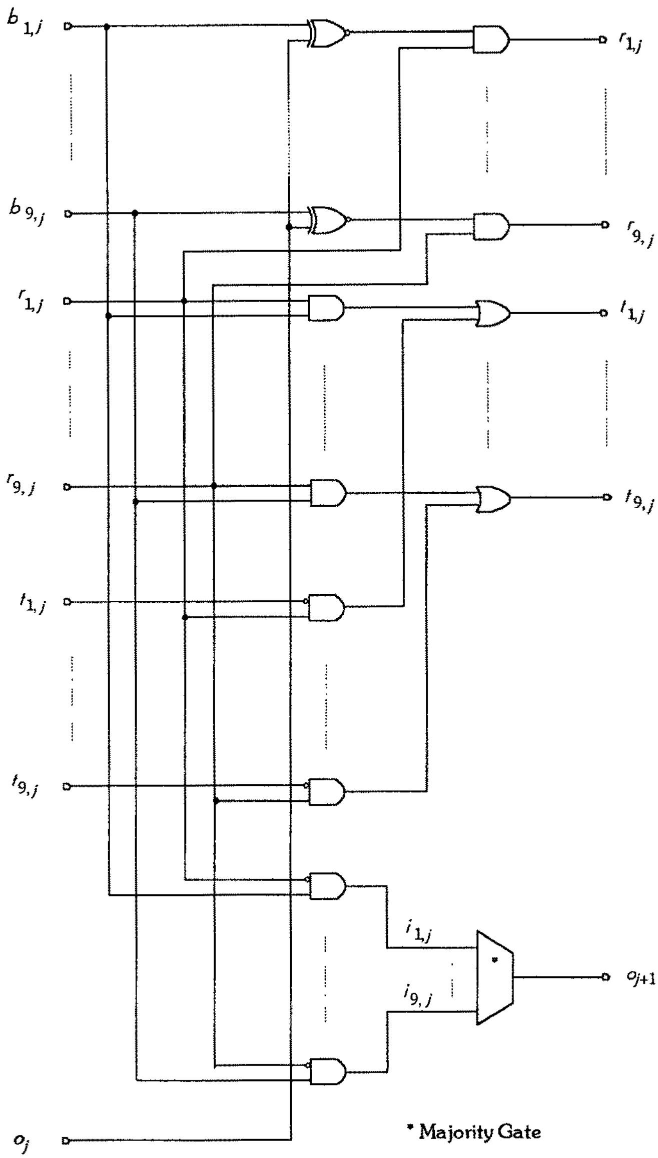

Fig. 4. The basic processing element (PE).

4 Conclusions

A new technique for realization of soft morphological filtering based on the modification of the majority gate has been presented in this paper. A pipelined systolic array architecture based on this technique has been also presented. The processing times of the proposed hardware structure are independent of the data window size and its hardware complexity grows linearly with the number of its inputs.

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