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An ASIC for fast grey-scale dilation

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Abstract

The design and VLSI implementation of a new ASIC which performs the operation of grey-scale dilation using both image and structuring element threshold decomposition is presented in this paper. The minimum rate of external operations of this ASIC is 30 MPix/sec and it can handle 3 × 3 pixel images and structuring elements of up to 4-bit resolution. The high speed of operation is achieved using the pipelining technique. The ASIC is implemented using a DLM, 1.0 μm, N-well, CMOS process provided by the European Silicon Structures (ES2), and it occupies a silicon area of 5.48 × 5.77 mm = 31.61 mm^2. It is intended to be used in machine vision applications, where the need for short processing times is crucial (e.g. robotics and military systems).

Keywords: Mathematical morphology; VLSI; ASIC

1. Introduction

Mathematical morphology is a methodology for image processing which is based on set theory and topology [1]. It offers a unified and powerful approach to numerous image processing problems, such as shape extraction, noise cleaning, thickening, thinning, skeletonising and object selection according to their size distribution. The two most basic morphological operations are dilation and erosion. These terms are derived from the Minkowski set algebra and correspond to the expansion and contraction of a binary region by one pixel around its boundary, respectively. Both are based on the use of a structuring element and associated with the structuring element is a reference pixel. The structuring element is sequentially translated through the image and compared with the region it overlays. Various structuring elements are used to perform mathematical morphology operations and are primarily dependent on the connectivity within the image. The concepts of binary morphology have been applied to grey-level images with great effect [2,3].

Specialised image processing machines, such as the cytocomputer, the image flow machine and the CLIP array processors have been built, which are capable of performing morphological operations [4,5]. These hardware architectures are limited to a fixed size structuring element. If the structuring element used in the morphological operations has a domain larger than the domain which the hardware can handle in one stage, then the structuring element must be decomposed into smaller structuring elements each of which is capable of being handled by one stage in the pipeline. Gerritsen and Verbeek [6] showed how convolution followed by a Look up Table operation can accomplish binary morphology operations. Zhuang and Haralick [7] described an algorithm for optimal structuring element decomposition. Shih and Mitchell [8] described an algorithm suitable for VLSI implementation, through which grey-scale morphological operations are decomposed into binary operations with the same dimensionality. Bhattachraya et al. [9] described an algebraic approach to morphological operations on 2D and 3D images. Grey-scale morphological operations are difficult to implement in real-time, unless they are decomposed into binary operations with the same dimensionality as the original operations.

This paper presents, for the first time, the design and VLSI implementation of an ASIC, suitable to perform the operation of dilation on grey-scale images, using both image and structuring element threshold decomposition. The ASIC can handle 3 × 3 pixel grey-level images and structuring elements of 4-bit resolution. Its frequency of operation is 30 MHz (worst case), its external rate of operation is 30 MPix/sec and its internal

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computational rate is 240 MIPS. The high speed of operation of this ASIC is achieved by pipelining the data. The design has been implemented using the SOLO 2040 VLSI CAD tool provided by ES2. The die size dimensions for the chip are 5.48×5.77 mm $= 31.61\ \text{mm}^2$, for a DLM, 1.0 μm, N-well, CMOS technology process. The usefulness of implementing this device is that the dilation operation is a necessary stage to a series of widely-used operations in image and signal processing, such as opening, closing, top-hat transform, region filling, detecting of connected components, textural segmentation and non linear edge detection using morphological gradient. Apart from processing binary images it will be useful in a great number of applications where the classification procedure ends in a relatively small number of classes (e.g. in remote sensing applications in analyses of geographical distribution of identifiable features, where the objects to be sorted are usually land, water, urbanisation, crops and forests). The ASIC is intended to be used in time critical applications. Real-time techniques are important not only in terms of improving productivity, but also in reducing operator errors associated with visual feedback delays.

2. Dilation and erosion

2.1. Binary dilation and erosion

Binary dilation and erosion are defined by means of Eq. (1) and Eq. (2), respectively [1,10]:

$$A \oplus B = \bigcup_{b \in B} (A)_b \tag{1}$$

$$A \ominus B = \bigcap_{b \in B} (A)_{-b} \tag{2}$$

where A and B are subsets of N-space (E^N) and $(A)_b$ is the translation of A by b.

Fast and simple hardware implementation of the above operations can be implemented through the following formulas:

$$(A \oplus B)_{(i,j)} = \text{OR}_{(m,n)}[A_{(i-m,j-n)} \text{ AND } B_{(m,n)}] \tag{3}$$

$$(A \ominus B)_{(i,j)} = \text{AND}_{(m,n)}[A_{(i+m,j+n)} \text{ OR } B_{(m,n)}] \tag{4}$$

where i, j, m and n are spatial coordinates.

2.2. Grey-scale morphology

The dilation z of grey level image f by structuring element k is defined as follows [8]:

$$\begin{aligned} z = {} & \{\{\vec{f}0 \oplus \vec{k}0\} + \{[\vec{f}1 \oplus \vec{k}0] \cup [\vec{f}0 \oplus \vec{k}1]\} \\ & + \ldots + \{[\vec{f}N \oplus \vec{k}0] \cup [\vec{f}(N-1) \oplus \vec{k}1] \\ & \cup \ldots \cup [\vec{f}1 \oplus \vec{k}(N-1)]\} \\ & + \ldots + \{[\vec{f}(M-1) \oplus \vec{k}(N-2)] \\ & \cup [\vec{f}(M-2) \oplus \vec{k}(N-1)]\} \\ & + \{[\vec{f}(M-1) \oplus \vec{k}(N-1)]\}\} \\ & - \vec{1} \end{aligned} \tag{5}$$

where $M-1$ and $N-1$ are the maximum grey-level values of the image and the structuring element, respectively. The terms of the threshold sequences $\vec{fj}$ and $\vec{kj}$ are defined by:

$$fj(i) = \begin{cases} 1 & \text{if } f(i) \geq j \\ 0 & \text{if } f(i) < j \end{cases} \quad \text{and} \quad kj(i) = \begin{cases} 1 & \text{if } k(i) \geq j \\ 0 & \text{if } k(i) < j \end{cases}$$

where j is the grey level value and i the spatial coordinate.

However, the structuring element is application dependent and, therefore, its maximum grey-level value is not known. In the case the structuring element is not fixed and since both the image and the structuring element are not zero, $\vec{f}0 = \vec{1}$, $\vec{k}0 = \vec{1} \Rightarrow \vec{f}0 \oplus \vec{k}0 = 1$,

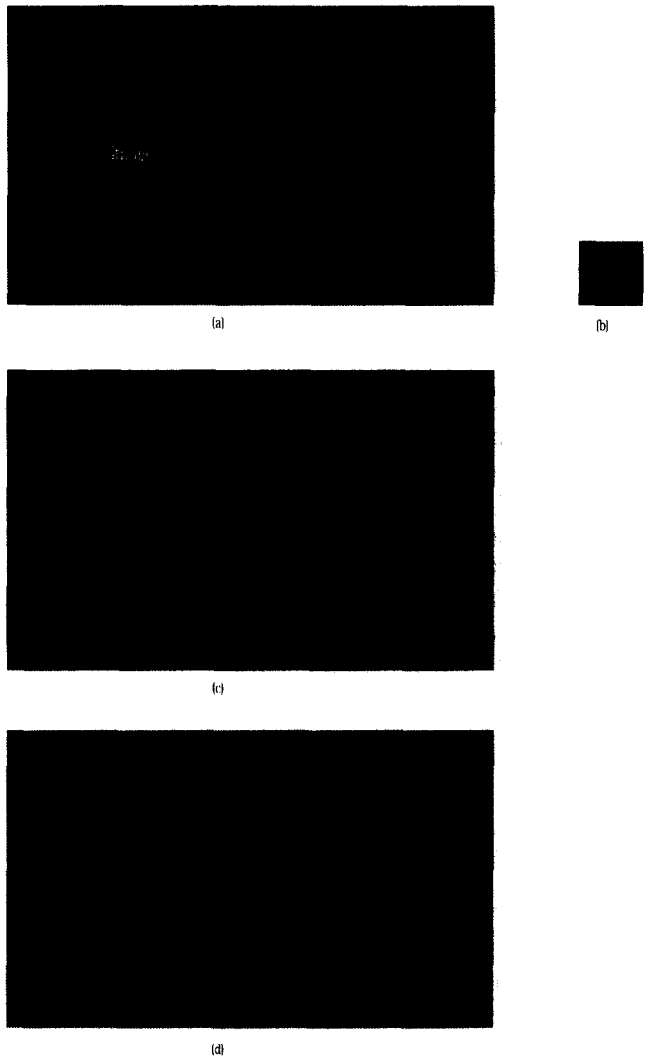


Fig. 1. Simulation results: (a) image, (b) structuring element (c) eroded image and (d) dilated previous image.

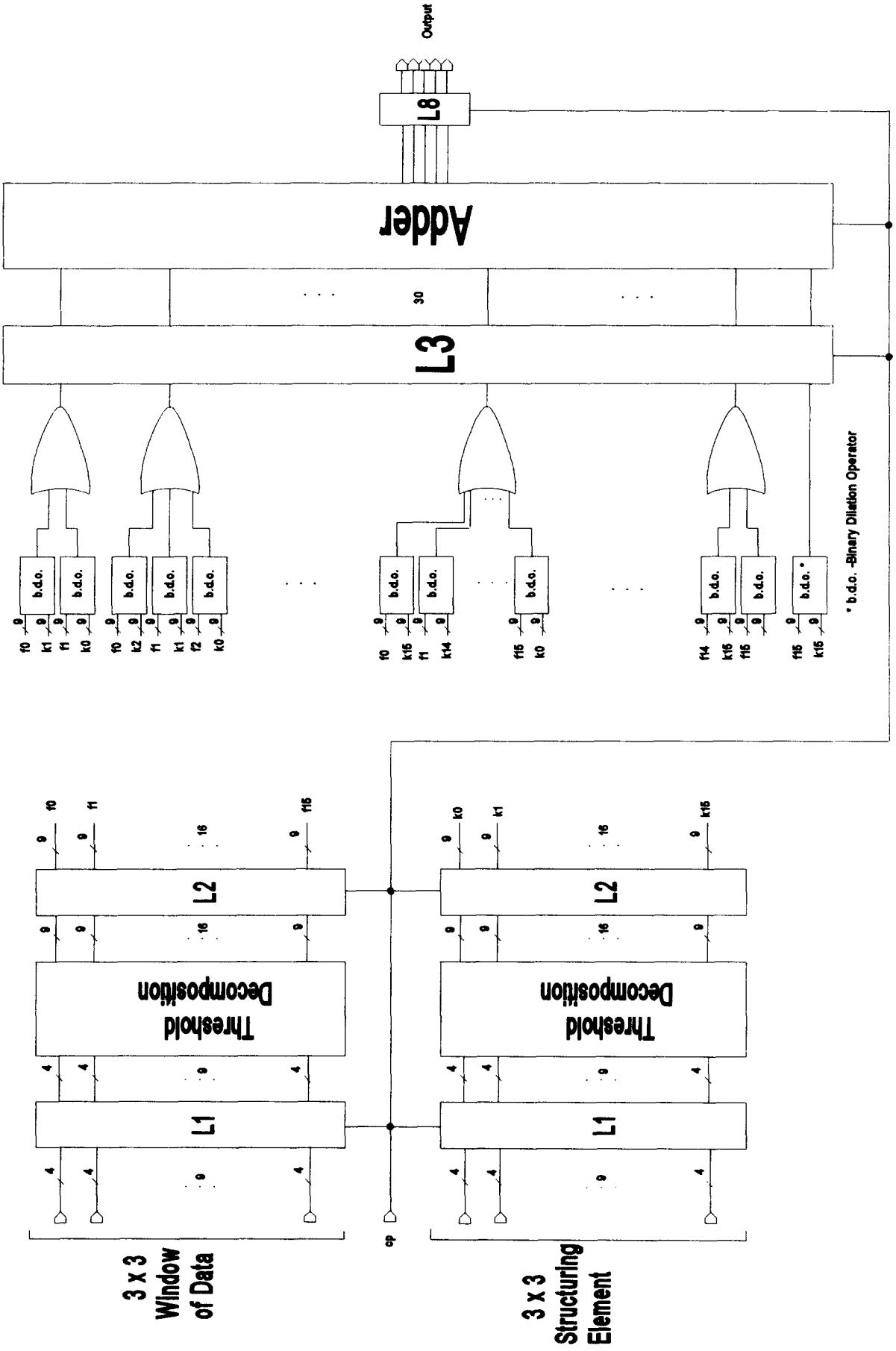


Fig. 2. Block diagram of the circuit of the ASIC.

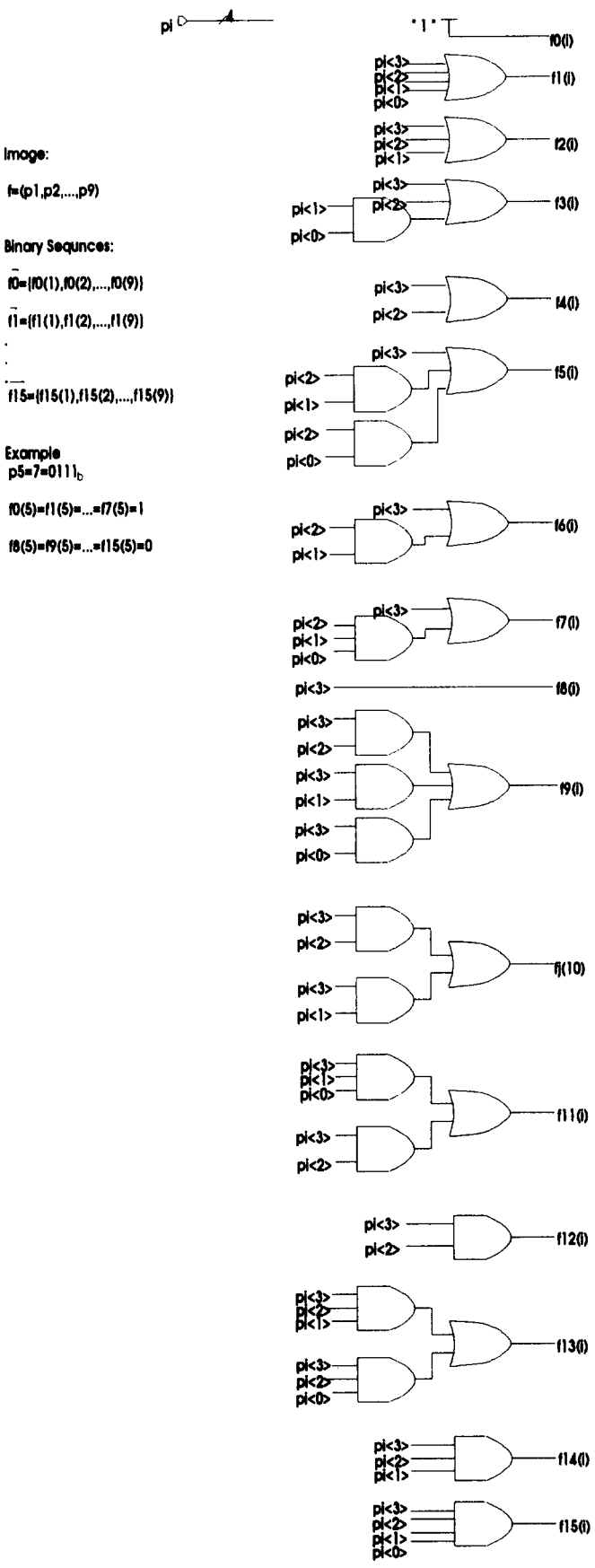


Fig. 3. Structure of the threshold decomposition circuit.

Eq. (5) can obtain the following form:

$$
\begin{aligned}
z = {} & \{\{[\vec{f}1 \oplus \vec{k}0] \cup [\vec{f}0 \oplus \vec{k}1]\} \\
& + \ldots + \{[\vec{f}N \oplus \vec{k}0] \cup [\vec{f}(N-1) \oplus \vec{k}1] \\
& \cup \ldots \cup [\vec{f}1 \oplus \vec{k}(N-1)]\} \\
& + \ldots + \{[\vec{f}(M-1) \oplus \vec{k}(N-2)] \\
& \cup [\vec{f}(M-2) \oplus \vec{k}(N-1)]\} \\
& + \{[\vec{f}(M-1) \oplus \vec{k}(N-1)]\}\} \qquad (6)
\end{aligned}
$$

The above derived equation has been used to design and VLSI implement an ASIC which performs the operation of grey-scale dilation.

Similarly the erosion y of f by k is:

$$
\begin{aligned}
y = {} & \{\{\vec{f}0 \ominus \vec{k}(N-1)\} \\
& + \{[\vec{f}1 \ominus \vec{k}(N-1)] \cap [\vec{f}0 \ominus \vec{k}(N-2)]\} \\
& + \ldots + \{[\vec{f}(M-1) \ominus \vec{k}(N-1)] \\
& \cap \ldots \cap [\vec{f}(M-N) \ominus \vec{k}0]\} \\
& + \ldots + [\vec{f}(M-1) \ominus \vec{k}0]\} - \vec{N} \qquad (7)
\end{aligned}
$$

Simulation results showing the usefulness of the dilation operation in a noise removal process from a grey-scale image are shown in Fig. 1.

3. Circuit description

The block diagram of the circuit of the ASIC is shown in Fig. 2. The pipeline technique has been adopted, since this allows complex operations to be performed in one clock cycle. The input data is a 3 × 3 pixel image window and a structuring element, each having a resolution of up to 4 bits. The data is latched in the first stage of the pipeline by means of two blocks of latches (L1) each block having size 9 × 4 bits. The data is then fed into the threshold decomposition circuit. This is basically a modified 4 to 16 line decoder. Each pixel p_i ($i = 0..8$) is decomposed in terms of binary sequences $fj(i)$ (see Eq. (5)) using the circuit shown in Fig. 3. The terms $fj(i)$ form

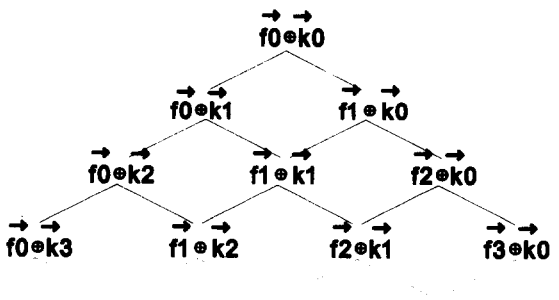


Fig. 4. Stacking property of binary dilations used to perform grey-scale dilation. Grey scale dilation is computed by obtaining the sum of the binary dilations of the same level.

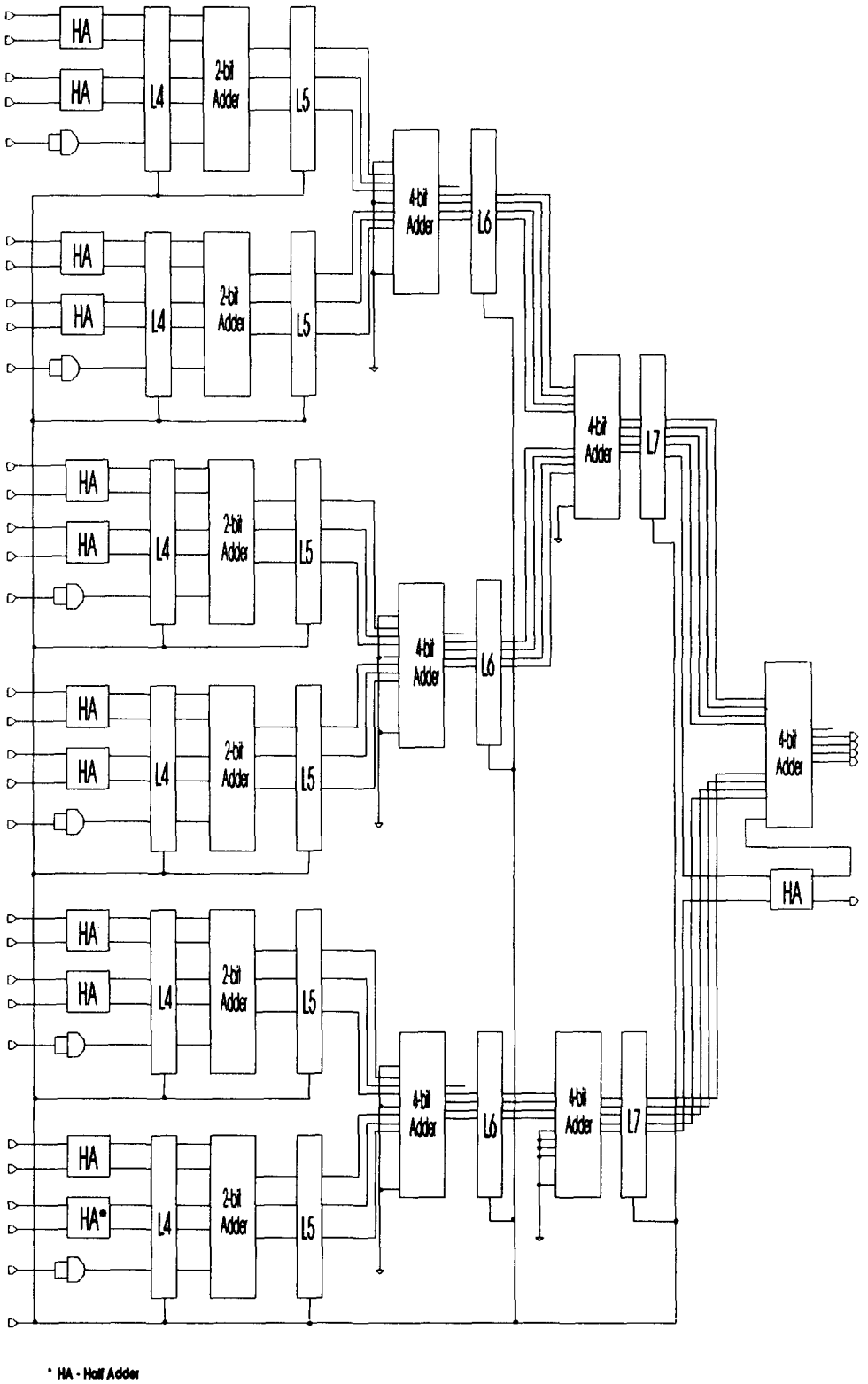


Fig. 5. Circuit diagram of the parallel/pipelined adder.

16 stacked binary sequences $\vec{f}j$ ($j = 0..15$), which are latched by means of two blocks of latches (L2), each block having size 16 × 9 bits (second stage of the pipeline). In the third stage of the pipeline the aforementioned sequences are combined in pairs (each pair consists of a binary image sequence $\vec{f}j$ and a binary structuring element sequence $\vec{k}j$). Then the operation of binary dilation is performed according to Eq. (3), using the neighbourhood of the central pixel of the image window. The outputs of these circuits are the inputs to

Table 1
Hardware requirements for 4-bit and 8-bit grey-scale dilation

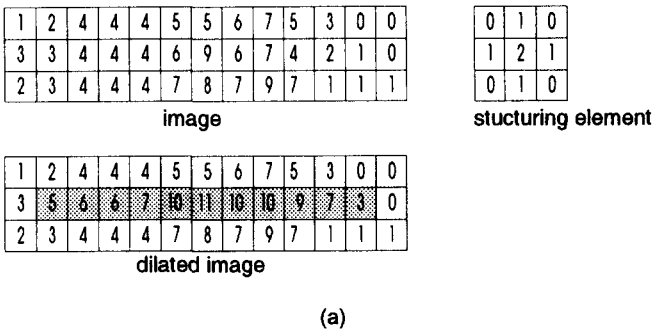
Element	4-bit Resolution	8-bit Resolution
L1	9 × 4 bits	9 × 8 bits
Binary sequences	16	256
L2	16 × 9 bits	256 × 9 bits
Binary dilation operators	$16^2 - 1$	$256^2 - 1$
OR gates	30	510
L3	30 bits	510 bits
Parallel/pipelined adder	4 stages	8 stages
L8	5 bits	9 bits

OR gates following Eq. (6) (union operation). The terms of the same level, as shown in Fig. 4, are the inputs to one OR gate. The outputs of these gates are collected by a 30-bit latch L3, since ($M - 1 = N - 1 = 15$), and they are used as the inputs to the parallel/pipelined adder, described in Fig. 5 (see Eq. (6)). The result of the addition is latched by 5-bit latch L8 in the last stage of the pipeline. The latter is the result of the dilation. Higher resolution images can be similarly treated. Table 1 shows the required sizes of the pipeline elements for 8-bit grey-scale images.

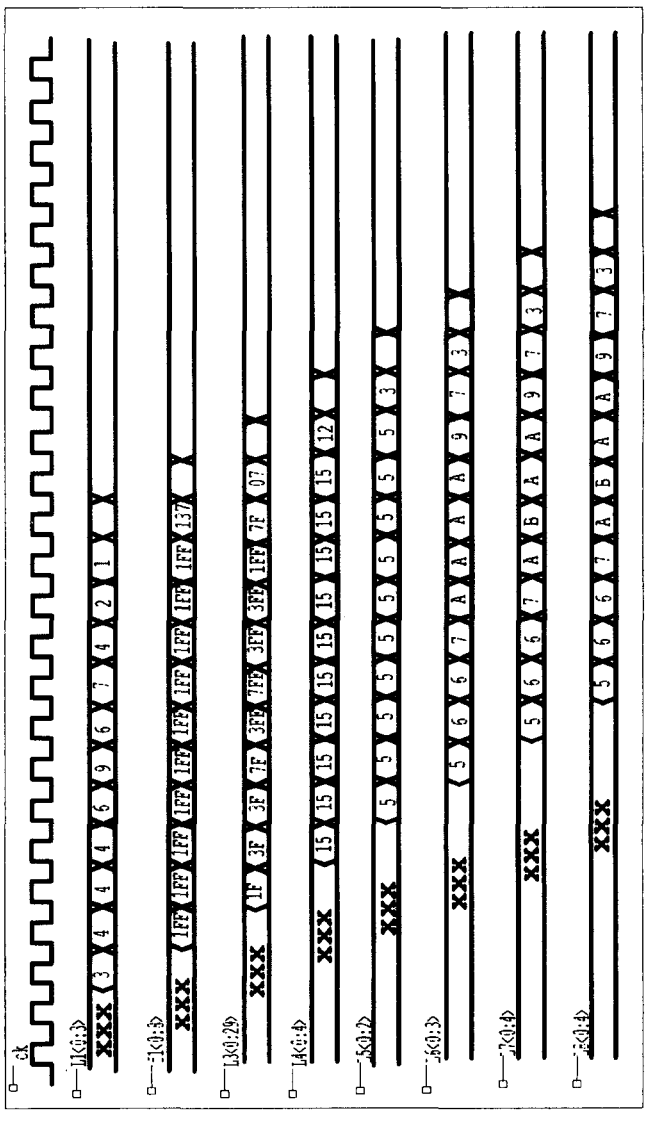
Similarly, the erosion operation can be implemented using Eq. (7). The process of image and structuring element decomposition is exactly the same as in the case of the dilation operation. The pair of binary sequences are now ordered according to Eq. (7) and the use of AND gates (instead of OR gates) is required in order to implement the intersection operation. Finally, the parallel/pipelined adder should employ an extra stage, where the subtraction of the offset term would be implemented.

4. VLSI implementation

A block level layout of the ASIC, including the pads, is shown in Fig. 6. The ASIC is divided into 33 rows onto which the standard cells have been built. The dimensions for the core of the chip are 4.63 × 4.91 mm = 22.73 mm^2 and the die size dimensions for the chip are 5.48 × 5.77 mm = 31.61 mm^2. The inputs to the ASIC are the 3 × 3 image and the structuring element (up to



(a)



(b)

Fig. 7. (a) Image, structuring element and dilated image across a horizontal line using the chip; (b) typical timing diagram of the pipeline circuitry, using the image and the structuring element of Fig. 7a.

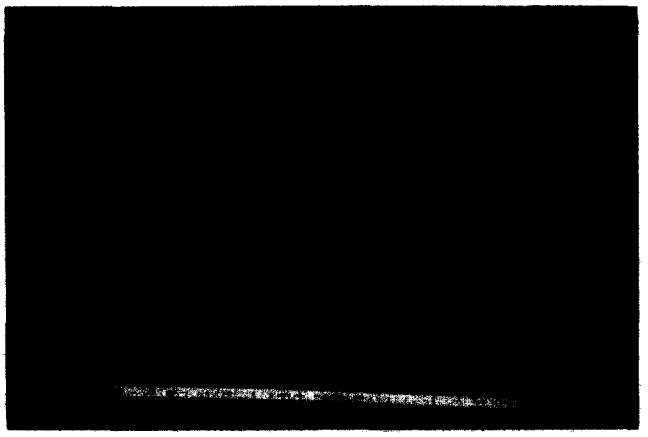


Fig. 6. Block level layout of the chip.

4-bit resolution), the clock, the power and ground connections, whereas the output is the 5-bit new pixel value.

The simulation and test language STL, a high level language, has been used to examine the functionality of the ASIC. Fig. 7a shows an image, a structuring element and the dilated image across a horizontal line using the chip. A typical timing diagram (using the image and the structuring element of Fig. 7a), including the values of the variables in the various stages, and showing the data flow across the pipeline circuitry is shown in Fig. 7b. The maximum frequency of operation (worst case) is 30 MHz, its external rate of operations is 30 MPix/sec and its internal computational rate of operations is $30 \times 8 = 240$ MIPS. Unless this ASIC is used this rate of operations could only be achieved with special purpose hardware.

5. Conclusions

The design and VLSI implementation of a new ASIC which performs fast grey-scale dilation using both image and structuring element threshold decomposition has been presented in this paper. It can handle 3×3 image windows and structuring elements of up to 4-bit resolution. Its frequency of operation is 30 MHz (worst case), its external rate of operations is 30 MPix/sec and its internal computational rate is 240 MIPS. With a DLM, 1.0 μm, N-well, CMOS technology process the die size dimensions for the chip are 5.48×5.77 mm $=$ 31.61 mm^2. Targeted applications include pattern recognition, robotics and military systems. Most of these applications are generally characterised by data throughput requirements that can only be met by dedicated hardware capable of operating in real-time.

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