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Non-linear image processing in hardware

A. Gasteratos[a], I. Andreadis[b,]*

[a]*Laboratory for Integrated Advanced Robotics, Department of Communication Computer and System Science, University of Genoa, Via Opera Pia 13, I-16145 Genoa, Italy*

[b]*Laboratory of Electronics, Section of Electronics and Information Systems Technology, Department of Electrical and Computer Engineering, Democritus University of Thrace, GR-671 00 Xanthi, Greece*

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Abstract

A new ASIC capable of computing rank order filters, weighted rank order filters, standard erosion and dilation, soft erosion and dilation, order statistic soft erosion and dilation, fuzzy erosion and dilation and fuzzy soft erosion and dilation is presented in this paper. Its function is based on local histogram and a successive approximation technique and performs on 3×3-pixel image windows. The hardware complexity of the proposed structure is linearly related to both image data window size and pixel resolution. The dimensions of the core of the proposed ASIC are $2.88\ \text{mm} \times 2.8\ \text{mm} = 8.06\ \text{mm}^2$ and its die size dimensions are $3.72\ \text{mm} \times 3.64\ \text{mm} = 13.54\ \text{mm}^2$. It executes 3.5×10^6 non-linear filter operations per second.

Keywords: Machine vision; Non-linear filters; Mathematical morphology; Fuzzy image processing; VLSI

1. Introduction

Non-linear filters are a large family of filters used in signal and image processing [1]. They include well-known filter classes such as rank order filters (median, min, max, etc.), morphological filters (e.g. opening, closing), etc. Rank order filters exhibit excellent robustness properties and provide solutions in many cases, where linear filters are inappropriate. Linear filters have poor performance in the presence of noise that is not additive as well as in cases where system non-linearities or non-Gaussian statistics are encountered [1]. Non-linear filters can suppress high frequency and impulse noise in an image, avoiding at the same time extensive blurring of the image, since they have good edge preservation properties. They have found numerous applications, such as in digital image analysis, speech processing and coding, digital TV applications, etc. Median and rank order filters are related to morphological filters [2,3]. It has been shown that erosions and dilations are special cases of rank order filters and that any rank order filter can be expressed either as a maximum of erosions or as a minimum of dilations [2]. Mathematical morphology offers a unified and powerful approach to numerous image processing problems, such as shape extraction, noise cleaning, thickening, thinning, skeletonizing and object selection according to their size distribution [4]. A relatively new approach to mathematical morphology is fuzzy mathematical morphology [5,6]. Several attempts made to apply fuzzy set theory to mathematical morphology, have resulted in different approaches and definitions. These are reviewed in Ref. [5], where a general framework is proposed. This framework leads to an infinity of fuzzy mathematical morphologies, which are constructed in families with specific properties.

Algorithms suitable for software implementation of rank order filters are tree sorts, shell sorts and quick sorts [1,7]. Most of these algorithms result in inefficient hardware structures, since they handle numbers in word-level. Several VLSI structures for median filters are studied in Ref. [8], where it is stated that for a relatively small pixel

* Corresponding author. Tel.: + 30-541-79566; fax: + 30-541-79564.

E-mail addresses: antonis@lira.dist.unige.it (A. Gasteratos), iandread@demokritos.cc.duth.gr (I. Andreadis)

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resolution the threshold decomposition technique is probably the best choice. Comparisons of VLSI architectures for weighted rank order filters are described in Ref. [9]. These include array architectures, stack filter architectures (threshold decomposition) and sorting network architectures. Comparisons are dependent on the choice of the filter parameters. It has been shown that the stack filter requires the largest silicon area since it depends exponentially on pixel resolution. For high pixel resolution and large window sizes, the sorting network is the best approach. Also, the stack filter is faster than the array architecture.

In this paper a new ASIC capable of computing rank order filters, weighted rank order filters, standard erosion and dilation, soft erosion and dilation [10,11], order statistic soft erosion and dilation [12], fuzzy erosion and dilation [6] and fuzzy soft erosion and dilation [13], is presented. It is based on local histogram and a successive approximation technique. The proposed hardware structure provides an output result in a fixed number of steps, which is equal to the image pixel resolution. Thus, the result does not depend on the local histogram values as it happens in the case of Gasteratos and Andreadis [14]. Image data window sizes are up to 3×3-pixels. It performs 3.5×10^6 non-linear filter operations per second. The die size dimensions of the ASIC are $3.72\ \text{mm}\times3.64\ \text{mm}=13.54\ \text{mm}^2$, for a 0.8 μm, DLM, CMOS technology process.

The rest of the paper is organized as follows. Definitions of the operations performed by the proposed ASIC are described in Section 2. The technique, on which the function of the ASIC is based, is discussed in Section 3. Hardware details, including the VLSI implementation and simulation results, are presented in Section 4. Concluding remarks are made in Section 5.

2. Basic definitions

Non-linear filters based on order statistics, which are computed by the proposed hardware structure, are the following:

- *Rank order filters* [1]. The input of such filters is a data window with an odd number of elements, N. These elements are shorted in ascending order and the output of the rank order filter with rank k is the kth element (kth order statistic). Special cases of rank order filters are the median, min and max filters.
- *Weighted rank order filters* [1]. This is a generalization of the previous category of filters. The output of a weighted rank order filter of rank k and weights $\{w_1, w_2, \dots w_N\}$ is kth order statistic of the set $\{w_1\diamond x_1, w_2\diamond x_2, \dots w_N\diamond x_N\}$, where w_i is a natural number and $w_i\diamond x_i$ denotes w_i times repetition of x_i.
- *Standard morphological filters* [4]. The basic morphological operations, from which all the other operations and filters are composed are erosion and dilation. These are defined as follows:

$$(f\ominus g)(x)=\min_{y\in\mathbb{G}}\{f(x+y)-g(y)\} \tag{1}$$

and

$$(f\oplus g)(x)=\max_{\substack{y\in\mathbb{G}\\ x-y\in\mathbb{F}}}\{f(x-y)+g(y)\}, \tag{2}$$

respectively, where $x, y\in\mathbb{Z}^2$ are the spatial co-ordinates, $f:\mathbb{F}\to\mathbb{Z}$ is the gray-scale image, $g:\mathbb{G}\to\mathbb{Z}$ is the gray-scale structuring element and $\mathbb{F}$, $\mathbb{G}\subseteq\mathbb{Z}^2$, are the domains of the gray-scale image and gray-scale structuring element, respectively.
- *Soft morphological filters* [11]. In soft morphological operations the max/min operations, used in standard morphology, are replaced by weighted order statistics. Furthermore, the structuring element is divided into two subsets; the core and the soft boundary. Soft morphological erosion and dilation are defined as follows:

$$f\ominus[\alpha,\beta,k](x)=\min_{\substack{(x+y)\in\mathbb{K}_1\\ (x+z)\in\mathbb{K}_2}}{}^{(k)}\left(\{k\diamond(f(y)-a(x+y))\}\cup\{f(z)-\beta(x+z)\}\right) \tag{3}$$

and

$$f\oplus[\alpha,\beta,k](x)=\max_{\substack{(x-y)\in\mathbb{K}_1\\ (x-z)\in\mathbb{K}_2}}{}^{(k)}\left(\{k\diamond(f(y)+a(x-y))\}\cup\{f(z)+\beta(x-z)\}\right), \tag{4}$$

respectively, where k is the order index, $\min^{(k)}$ and $\max^{(k)}$ are the kth smallest and the kth largest, respectively, x, y, $z\in\mathbb{Z}^2$, are the spatial co-ordinates, f: $\mathbb{F}\to\mathbb{Z}$ is the gray-scale image, a: $\mathbb{K}_1\to\mathbb{Z}$ is the core of the gray-scale structuring element, β: $\mathbb{K}_2\to\mathbb{Z}$ is the soft boundary of the gray-scale structuring element, $\mathbb{F}$, $\mathbb{K}_1$, $\mathbb{K}_2\subseteq\mathbb{Z}^2$ are the domains of the gray-scale image, the core of the gray-scale structuring element and the soft boundary of the gray-scale structuring element, respectively, and $\mathbb{K}_2=\mathbb{K}\backslash\mathbb{K}_1$, where $\mathbb{K}\subseteq\mathbb{Z}^2$ is the domain of the gray-scale structuring element.
- *Order statistic soft morphological filters* [12]. In this class the order index k and the repetition of the elements of the core are generally different. Order statistic soft morphological erosion and dilation are defined as follows:

$$f\ominus[\alpha,\beta,k,r](x)=\min_{\substack{(x+y)\in\mathbb{K}_1\\ (x+z)\in\mathbb{K}_2}}{}^{(k)}\left(\{r\diamond(f(y)-a(x+y))\}\cup\{f(z)-\beta(x+z)\}\right) \tag{5}$$

and

$$f\oplus[\alpha,\beta,k,r](x) = \min^{(k)}_{\substack{(x-y)\in\mathbb{K}_1\\(x-z)\in\mathbb{K}_2}} (\{r\Diamond(f(y)+a(x-y))\} \cup\{f(z)+\beta(x-z)\}), \quad (6)$$

respectively, r is the repetition times of the results related to the core of the structuring element. The other variables are exactly the same with those in Eqs. (3) and (4).

- *Fuzzy morphological filters* [6]. In this approach, mathematical morphology is studied in terms of fuzzy fitting. The fuzziness is introduced by the degree to which the structuring element fits into the image. Fuzzy erosion and dilation are defined as follows:

$$\mu_{A\ominus B}(x) = \min\left[1, \min_{y\in B}[1+\mu_A(x+y)-\mu_B(y)]\right], \quad (7)$$

$$\mu_{A\oplus B}(x) = \max\left[0, \max_{y\in B}[\mu_A(x-y)+\mu_B(y)-1]\right], \quad (8)$$

respectively, where $x, y\in\mathbb{Z}^2$ are the spatial co-ordinates and μ_A, μ_B are the membership functions of the image and the structuring element, respectively.

- *Fuzzy soft morphological filters* [13]. Here fuzzy fitting is introduced into soft morphology. Fuzzy soft erosion and dilation are defined as follows:

$$\mu_{A\ominus[B_1,B_2,k]}(x) = \min[1, \min^{(k)}_{\substack{y\in B_1\\z\in B_2}}(\{k\Diamond(\mu_A(x+y)-\mu_{B_1}(y)+1)\} \cup\{\mu_A(x+z)-\mu_{B_2}(z)+1\})], \quad (9)$$

$$\mu_{A\oplus[B_1,B_2,k]}(x) = \max[0, \max^{(k)}_{\substack{y\in B_1\\z\in B_2}}(\{k\Diamond(\mu_A(x-y)+\mu_{B_1}(y)-1)\} \cup\{\mu_A(x-z)+\mu_{B_2}(z)-1\})], \quad (10)$$

respectively, where $\mu_A, \mu_{B1}, \mu_{B2}$ are the membership functions of the image, the core and the soft boundary of the structuring element.

Additionally, for the fuzzy structuring element $B\subset\mathbb{Z}^2 : B = B_1\cup B_2$ and $B_1\cap B_2 = \emptyset$.

3. Algorithm description

In this section an algorithm which computes any weighted order statistic is described [14]. It is based on a local histogram technique [15,16]. According to this any order statistic can be found by summing the values in the histogram until the desired order statistic is reached. The number of steps of this process depends on the values of the local histogram. Here, instead of adding the local histogram values serially, a successive approximation technique has been adopted. This ensures that the result is traced in a fixed number of steps. The number of steps is equal to the number b of bits per pixel. According to the successive approximation technique the N pixel values are initially compared with 2^{b-1}. Pixel values, which are greater than, less than or equal to that value are marked with labels GT, LT and EQ, respectively. GT, LT and EQ are either 0 or 1. Pixel labels are then multiplied by the corresponding pixel weight. The sum of the LTs and EQs determines whether the kth order statistic is greater than, less than or equal to 2^{b-1}. More specifically:

(i) If the sum $\sum_{j=1}^{N} w_j(\mathrm{EQ}_j + \mathrm{LT}_j)$ is greater than or equal to k and the sum $\sum_{j=1}^{N} w_j\mathrm{LT}_j$ is less than k, then the kth order statistic is 2^{b-1}.
(ii) If the sum $\sum_{j=1}^{N} w_j\mathrm{LT}_j$ is greater than or equal to k, then the kth order statistic is less than 2^{b-1} and, therefore, 2^{b-2} should be subtracted from 2^{b-1}.
(iii) Otherwise, the kth order statistic is greater than 2^{b-1} and, therefore, 2^{b-2} should be added to 2^{b-1}.

If the kth order statistic is not traced according to (i), then the comparison of each pixel value is made with the subtraction or addition result of (ii) or (iii), respectively. This is called temporal result (temp); when condition (i) is valid the kth order statistic is equal to temp. The process is repeated until the required weighted order statistic is computed. In the ith step number 2^{b-1-i} is either subtracted or added to temp. Thus, the kth order statistic is computed in b steps (worst case). In the common case of 8-bit image pixel resolution, the local histogram summation algorithm [16] requires 1 to $2^8 - 1 = 255$ (worst case) steps to compute an order statistic, whereas the described algorithm requires 1 to 8 steps. In general, the number of steps in the first case is exponentially related to the pixel resolution, i.e. there is a relationship $O(2^b)$. In the second case this relationship becomes linear (O(b)).

Table 1 presents an illustrative example of the proposed algorithm application to a five pixel data window of 4-bit resolution with weights: $w_1 = 1$, $w_2 = 3$, $w_3 = 5$, $w_4 = 3$, $w_5 = 1$. The 4th largest element (max [4]) of this window is searched; this is the 10th order statistic and, therefore, $k = 10$.

4. Design and implementation of the proposed hardware structure

The block diagram of the proposed hardware structure is shown in Fig. 1. The pipeline principle is used in the entire process. Its inputs are a 1-byte data bus, the selection bits S_1, S_0 of the input demultiplexer, the reset and

Table 1
An illustrative example of the algorithm use

	Image pixels							
i	2	1	5	10	7	Temp	Condition	Output
1	LT	3*LT	5*LT	3*GT	LT	8	$\sum_{j=1}^{5} w_j \mathrm{LT}_j \geqslant 10 \Rightarrow$ SUB	0
2	LT	3*LT	5*GT	3*GT	GT	4	$\sum_{j=1}^{5} w_j \mathrm{LT}_j < 10 \Rightarrow$ ADD	0
3	LT	3*LT	5*LT	3*GT	GT	6	$\sum_{j=1}^{5} w_j \mathrm{LT}_j < 10 \Rightarrow$ ADD	0
4	LT	3*LT	5*LT	3*GT	EQ	7	$\sum_{j=1}^{5} w_j (\mathrm{EQ}_j + \mathrm{LT}_j) \geqslant 10$ AND $\sum_{j=1}^{5} w_j \mathrm{LT}_j < 10$	7

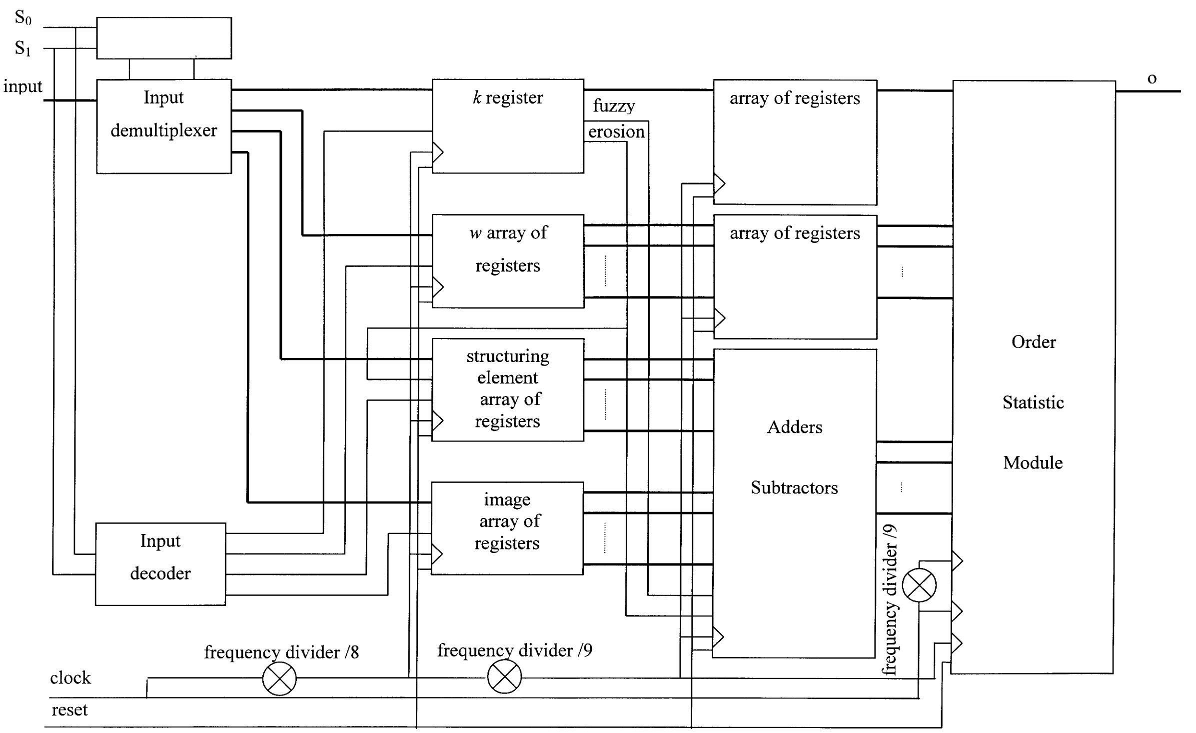
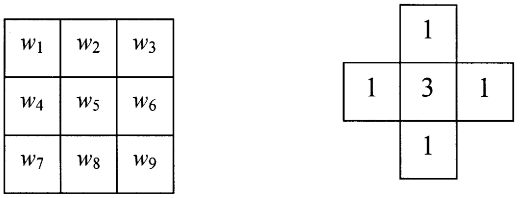


Fig. 1. Block diagram of the proposed hardware structure.

the clock signals. The states of the selection bits of the demultiplexer determine the type of input loaded. More specifically, for $S_1S_0 = 00$ 1 byte of control data is loaded. Its two most significant bits (MSBs) determine whether the operation is fuzzy or not and whether the operation is erosion or dilation. The other bits correspond to the order index k. Table 2 presents the hexadecimal control codes of this byte for some representative operations. This byte is stored into an 8-bit register with parallel load (k register). The input decoder controls the load input of this register. When $S_1S_0 = 01$ nine bytes are loaded serially. These correspond to the weights of the 3×3-pixel neighborhood and are stored into the w array of registers. This array is a serial to parallel module consisting of nine 8-bit registers with parallel load and it is also controlled by the input decoder. If a smaller than a 3×3-pixel image window is to be processed, then pixels which are not taken into account are considered to have zero weights. In standard rank order filters and morphological operations the weights are equal to 1. Fig. 2 depicts an example of a cross-shaped neighborhood, with central pixel weight equal to 3. In

Table 2
Hexadecimal control codes for some representative operations performed by the proposed ASIC

Operation	Hexadecimal code
Median	05
Center weighted median ($w = 3$)	06
Max	09
Standard dilation	09
Min	01
Standard erosion	41
Soft dilation ($k = 3$, the core of the structuring element is the central pixel)	0B
Soft erosion ($k = 3$, the core of the structuring element is the central pixel)	41
Fuzzy dilation	89
Fuzzy erosion	C1
Fuzzy soft dilation ($k = 3$, the core of the structuring element is the central pixel)	8B
Fuzzy soft erosion ($k = 3$, the core of the structuring element is the central pixel)	Cl



w_1=0, w_2=1, w_3=0, w_4=1, w_5=3, w_6=1, w_7=0, w_8=1, w_9=0,

Fig. 2. Example of weights consideration.

soft and fuzzy soft morphological operations the weights of core pixels are equal to the order index and the weights of soft boundary pixels are 1. When $S_1 S_0 = 10$ the nine bytes of the structuring element are loaded serially. These are stored into the structuring element array of registers, which has a similar structure with the w array of registers. The sequence of structuring element pixel loading is shown in Fig. 3. In non-morphological operations (rank order and weighted rank order operations) the values of the structuring element pixels are 0. Finally, when $S_1 S_0 = 11$ the image pixels are loaded into the image array of registers. Every nine clock pulses one 3×3-pixel image area is loaded. The original clock frequency is 250 MHz. The data loading frequency is extracted by dividing the original clock by eight through a frequency divider (Fig. 1). This lower frequency is further divided by nine and it is used as the clock input to the rest of the process, but to the order statistic module. The two lower frequencies are used to synchronize image data loading (nine pixels) and order statistic module operations (eight steps of processing). The next stage of the circuit is the adders/subtractors module. The block diagram of this module is shown in Fig. 4. The pixels of the image and the structuring element are latched by means of 18 registers. The outputs of the registers are fed into nine adders/subtractors. These, depending on the operation (dilation/erosion), add/subtract the image pixels with the corresponding structuring element pixels. In the next stage, provided that the operation is fuzzy, number FF is subtracted or added in the case of dilation or erosion, respectively, according to Eqs. (7)–(10). For normalized pixel values [17] this number corresponds to 1. If the operation is not fuzzy, then 00 is subtracted or added and, therefore, the result is not affected. Since the addition results of dilation and fuzzy erosion may be greater than FF and the subtraction results of erosion and fuzzy dilation may be less than 00, the results are limited, through a clipper module, in the range [00..FF]. This module tests the MSB of the result and outputs either FF or 00 for each of the aforementioned overflow cases. The results are then fed into the order statistic module. The order index k and the weights, properly delayed through registers are also inputs to this module.

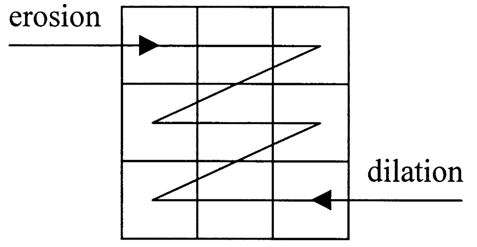


Fig. 3. Structuring element pixel loading in the cases of erosion and dilation.

The block diagram of the order statistic module is shown in Fig. 5. It consists of nine pipeline stages. A non-linear computation operation is completed in eight successive steps. In each of these steps the value of the intermediate 8-bit signal temp is changed to (temp $\pm\, 2^{b-1-i}$), according to the algorithm. This is achieved through a feedback loop (Fig. 5). The addition/subtraction results are compared concurrently with signal temp by means of nine comparators. Each of these comparators has two outputs, determining whether the addition/subtraction result is less than or equal to signal temp. Thus, labels LT and EQ are extracted and latched through 18 flip-flops (F/F). Then, these labels are

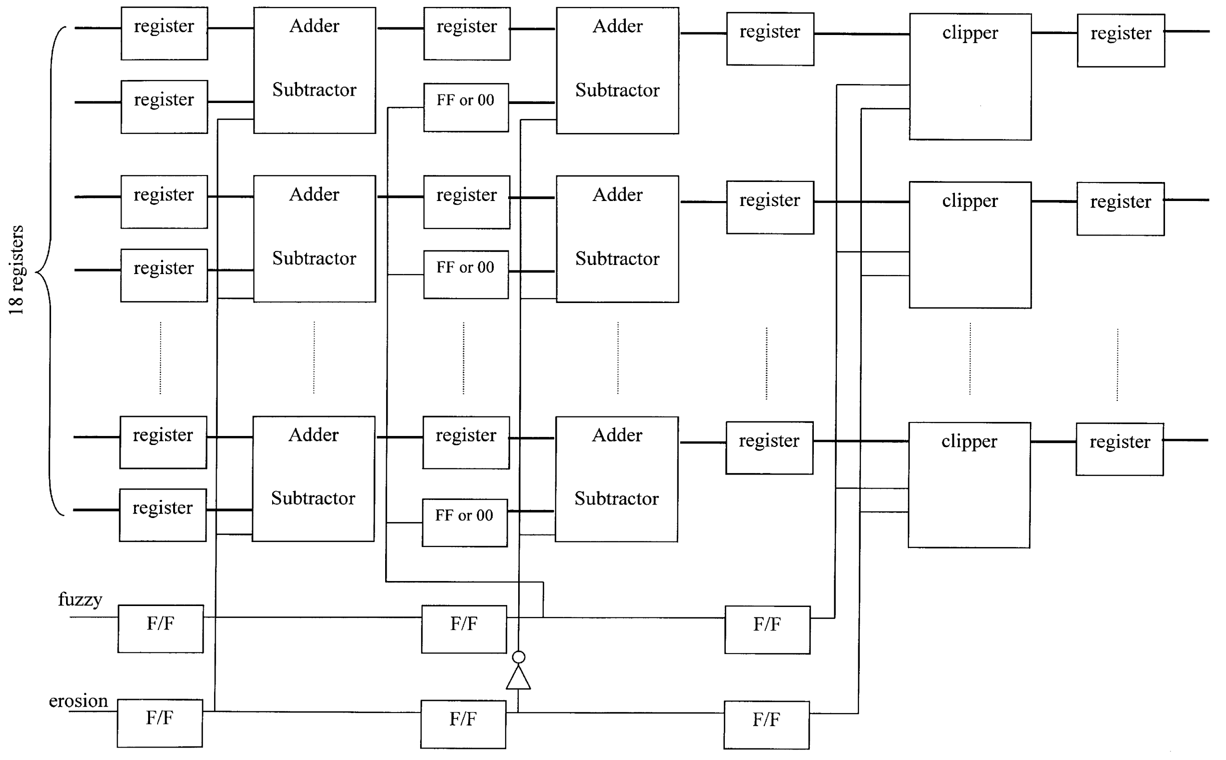


Fig. 4. Adders/Subtractors module.

multiplied with the corresponding weights (according to the algorithm) through an array of 18 multipliers (II). Since labels are 1-bit long, each of these multipliers is an array of 2-input AND gates. The first input of each AND gate is the label and the second a bit of the binary representation of the weight. The multiplication results are collected by means of 18 registers (R). In the next stages the sums $\sum_{j=1}^{N} w_j \mathrm{EQ}_j$ and $\sum_{j=1}^{N} w_j \mathrm{LT}_j$ are formed, by means of two parallel tree adders ($\boldsymbol{\Sigma}$), each consisting of three pipeline stages; the sum $\sum_{j=1}^{N} w_j(\mathrm{EQ}_j + \mathrm{LT}_j)$ is formed through a 6-bit adder. The results $\sum_{j=1}^{N} w_j (\mathrm{EQ}_j + \mathrm{LT}_j)$ and $\sum_{j=1}^{N} w_j \mathrm{LT}_j$ are compared with the order index k, by means of two comparators. If the logical product of the comparators outputs is 1, then the result has been found. If it is so or the result has been found on a previous step (this is denoted by the internal signal found), then no further addition or subtraction is required. Signal found controls the multiplexer that provides to the adder/subtractor either 00 or 2^{b-1-i}, in the cases of finding the result or not, respectively. Number 2^{b-1-i} is obtained by means of a b-state counter. The states of the counter are powers of 2 in descending order. The inverted output of the second comparator denotes that $\sum_{j=1}^{N} w_j \mathrm{LT}_j \geqslant k$. This controls the operation of the adder/subtractor, through the internal signal add_sub. The result of the addition/subtraction is the new value of signal temp and it is stored into register R* (Fig. 5). Registers R* and R** are triggered by the original clock divided by nine and by 72, respectively; the rest part of order statistic module (registers R) is triggered by the original clock. Therefore, in nine clock pulses of the original clock the new temp value is computed. In order to compute the output value o, $8 \times 9 = 72$ clock pulses of the original clock are required (the number of steps that are required for the computation of the output is eight).

4.1. VLSI implementation

The Cadence DFWII VLSI CAD tool with the AMS hit-kit 2.40 have been used to design and implement the ASIC. It has been implemented using a 0.8 μm, DLM, CMOS technology. A microphotograph of the ASIC, is shown in Fig. 6. The core dimensions of the chip are $2.88\ \mathrm{mm} \times 2.8\ \mathrm{mm} = 8.06\ \mathrm{mm}^2$ and its die size dimensions are $3.72\ \mathrm{mm} \times 3.64\ \mathrm{mm} = 13.54\ \mathrm{mm}^2$. The inputs to the ASIC are the 8-bit data input, selection signals S_1 and S_2, the clock and the reset signals, the power and ground connections for both the core and the periphery of the chip, whereas the output is the 8-bit computed

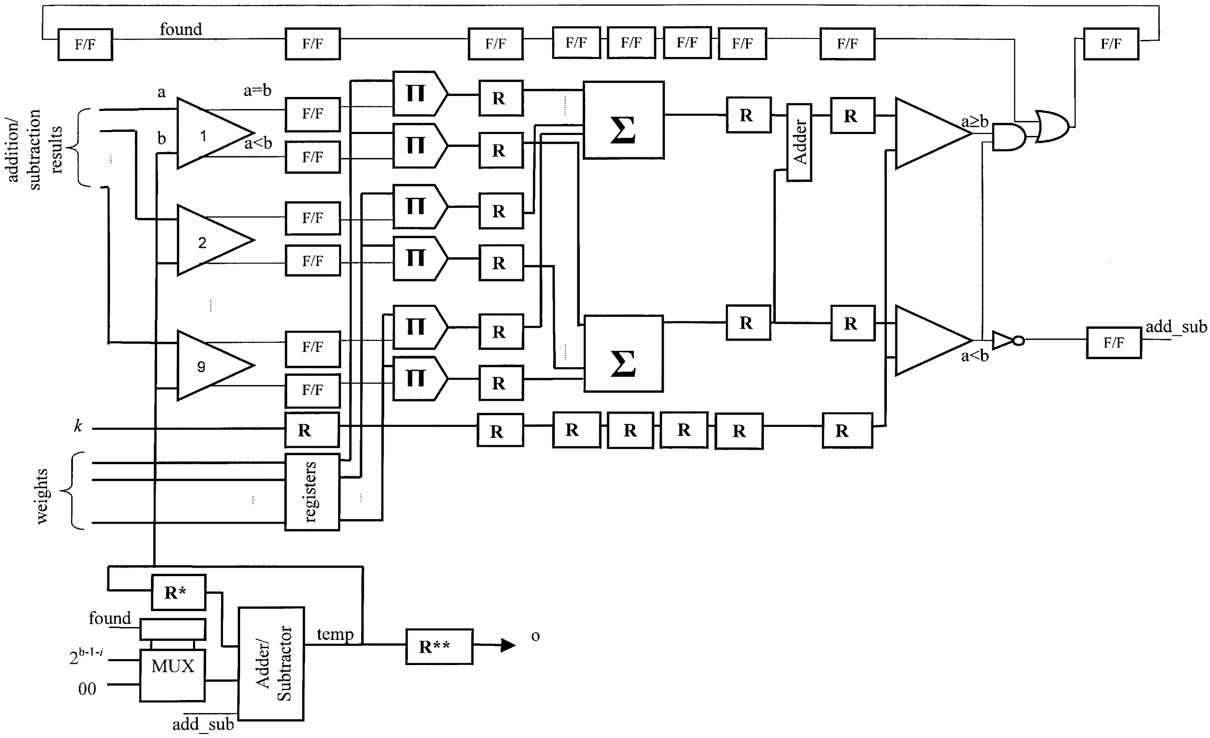


Fig. 5. Order statistic module.

value. The simulation and test language STL, a high level language, has been used to examine the functionality of the ASIC. Its maximum frequency of operation is 3.5 MHz. A typical timing diagram, including the values of the variables in the various stages is presented in Fig. 7. In this figure three cycles of the proposed successive approximation technique are demonstrated. The first line is the original clock divided by nine and this triggers the counter. The eight states of the counter are shown in the second line of the diagram. The next line represents signal found. When this signal is set to "1" the output of the multiplexer is set to 00 (next line). The operation of addition/subtraction is controlled by signal add_sub (next line). When this is "1", then the output of the multiplexer is subtracted from the previous temp value (next line), otherwise it is added. The next line shows the original clock divided by 72 and this triggers the output register R**. The final output is obtained when the order statistic module has completed the required eight steps.

The structure presented in this section is scaleable both in terms of pixel resolution and size of image window. For higher pixel resolution the circuit should be expanded linearly to accommodate the new pixel representation. Furthermore, additional steps will be needed in the order statistic module (equal to the additional number of bits in image pixel resolution representation). For larger size image windows additional registers to store data and adders/subtractors and comparators for the arithmetic operations are required. The ASIC can operate faster (approximately eight times), by utilizing eight order statistic modules consequently in pipeline fashion. Also, for an even faster operation the image data window could be loaded in parallel. This hardware module would perform $8 \times 9 = 72$ times faster approximately.

5. Conclusions

A new ASIC suitable for performing non-linear image processing operations has been presented in this paper. It is based on local histogram and a successive approximation technique. This ASIC performs on 3×3-pixel image windows and computes rank order filters, weighted rank order filters, standard erosion and dilation, soft erosion and dilation, order statistic soft erosion and dilation, fuzzy erosion and dilation and fuzzy soft erosion and dilation. The die size dimensions for the chip are $3.72\ \text{mm} \times 3.64\ \text{mm} = 13.54\ \text{mm}^2$, for a 0.8 μm, DLM,

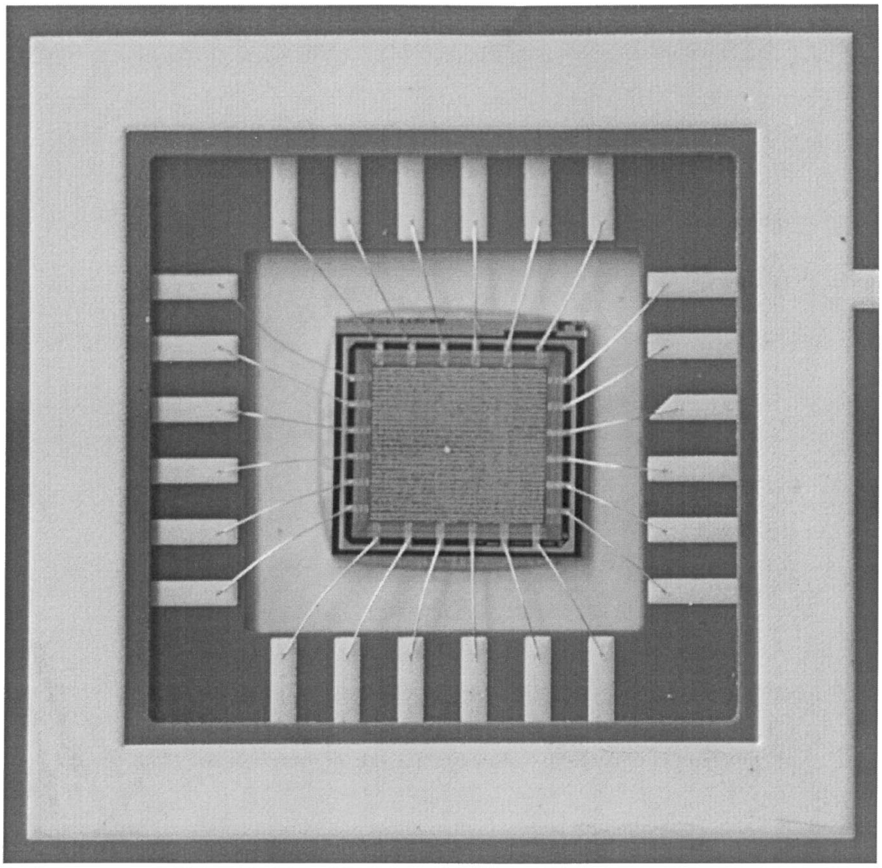


Fig. 6. A microphotograph of the proposed ASIC.

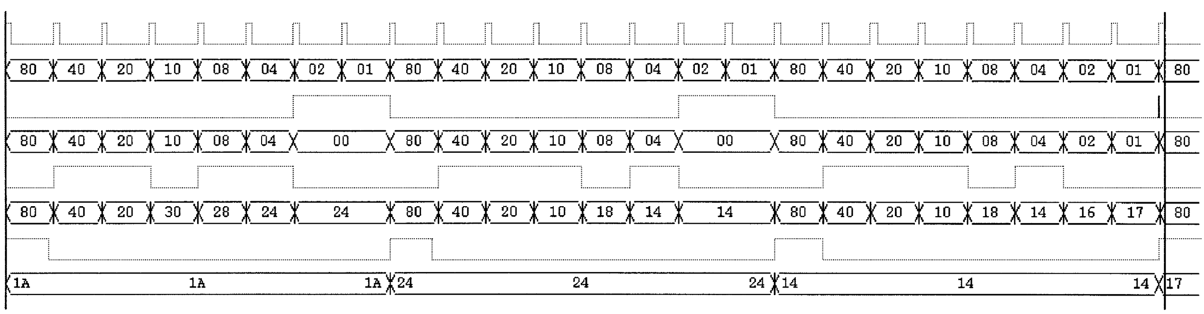


Fig. 7. Demonstration of the successive approximation technique.

CMOS technology process. It performs 3.5×10^6 non-linear filter operations per second. The architecture of the ASIC is scaleable both in terms of pixel resolution and image window size and its hardware complexity is linearly related to both of them.

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About the Author—ANTONIOS GASTERATOS received the Diploma and the Ph.D. degrees from the Department of Electrical and Computer Engineering, Democritus University of Thrace, Greece, in 1994 and 1999, respectively. He is currently a post-doc fellow in the Laboratory for Integrated Advanced Robotics, Department of Communication, Computer and System Science, University of Genoa, Italy, with a TMR (EU) grand. His research interests include computer vision, fuzzy and non-linear image processing, digital VLSI design and computer architectures. He is a member of the Technical Chamber of Greece (TEE).

About the Author—IOANNIS ANDREADIS received the Diploma Degree from the Department of Electrical Engineering, DUTH, Greece, in 1983, and the M.Sc. and Ph.D. degrees from the University of Manchester Institute of Science and Technology (UMIST), UK, in 1985 and 1989, respectively. His research interests are mainly in machine vision and VLSI-based computing architectures for machine vision. He joined the Department of Electrical and Computer Engineering, DUTH, in 1992. He is a member of the Editorial Board of the Pattern Recognition Journal, the Technical Chamber of Greece (TEE) and the IEEE.