A CO-DESIGN METHODOLOGY FOR IMPLEMENTING COMPUTER VISION ALGORITHMS FOR ROVER NAVIGATION ONTO RECONFIGURABLE HARDWARE

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ABSTRACT

Vision-based robotics applications have been widely studied in the last years. However, up to now solutions that have been proposed were affecting mostly software level. The SPARTAN project focuses in the tight and optimal implementation of computer vision algorithms targeting to rover navigation. For evaluation purposes, these algorithms will be implemented with a co-design methodology onto a Virtex-6 FPGA device.

INTRODUCTION

The exploration of Mars is one of the main goals for both NASA and ESA, as confirmed by past and recent activities. The last 15 years there are a number of on-orbit and surface missions to Mars with remarkable results. The impressive success of previous missions (NASA's Mars Global Surveyor, Mars Odyssey, Phoenix, Mars Reconnaissance Orbiter, as well as ESA's Mars Express) enables a continued investment of efforts in this direction, and also facilitating international discussion for joint Mars exploration missions between ESA and NASA, such as in case of ExoMars which is scheduled for 2018 [3].

Autonomous robots' behavior greatly depends on the accuracy of their decision-making algorithms. Vision-based solutions are becoming more and more attractive due to their decreasing cost, as well as their inherent coherence with human imposed mechanisms. In the case of stereo vision-based navigation, the accuracy and the refresh rate of the computed disparity maps are the cornerstone of success. However, robotic applications place strict requirements on the demanded speed and accuracy of vision depth-computing algorithms.

In order to support this goal, at this project we aim to provide a sufficient implementation of computer vision algorithms for rover navigation. Rather than similar approaches that solve this problem solely in software-level, our objective is to provide a number of computer vision algorithms in ESA compatible VHDL format, whereas the implementation of SPARTAN system will be performed using a co-design methodology and a Virtex-6 FPGA device.

The rest of the paper is organized as follows: Section II describes the employed computer vision algorithms for the SPARTAN system, whereas section III discusses the implementation of these algorithmic approaches. Finally, conclusions are summarized in section IV.

COMPUTER VISION ALGORITHMS FOR SPARTAN SYSTEM

The main objective of our solutions is to achieve the desired rover navigation function, while reducing as much as possible the required overall budgets. For this purpose, a number of novel computer vision algorithms will be developed both in C/C++, as well as VHDL language.

A schematic view of the proposed solution is depicted in Figure 1. More specifically, the computer vision algorithms that will be implemented during the SPARTAN project are summarized as follows:

- Imaging: Implementing suitable local image processing that can serve image products.
- Visual Odometry: Provide an estimation of the displacement of the rover.
- Visual SLAM: Determine the current location of the rover.
- 3D Map reconstruction: Reconstruct the 3Dimensional shape of the terrain being imaged in front of the rover.
- Localization: Locates the new spatial location of rover at the map.

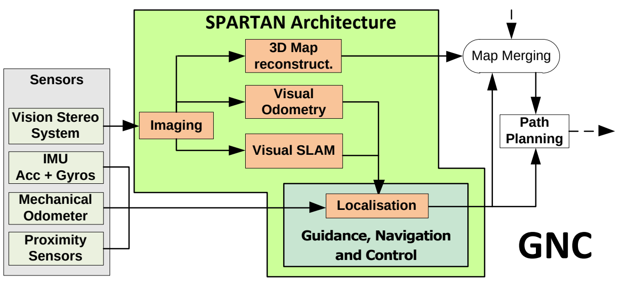

Fig. 1. SPARTAN function identifications.

Since our goal is to achieve an efficient implementation of these algorithms, special care should be applied both during the selection of them, as well as at their development. Furthermore, in order to achieve additional performance improvement, a number of source-to-source modifications might be applied. For this purpose, well established tools, already developed from NTUA [1], will be employed.

PHYSICAL IMPLEMENTATION

The implementation of computer vision algorithms will be performed into VHDL description, while all the ESA requirements/guidelines will be meeting [2]. The purpose of these guidelines is to ensure a good coding standard for VHDL, w.r.t. to readability, portability and a high level of verification. Detail stages for system development (e.g. VHDL models for component simulation, board-level simulation, system-level simulation and test-benches) will be also described.

The target platform for our study is Xilinx Virtex-6 FPGA device. Furthermore, during the SPARTAN activity we will analyze the efficiency of design implementation into such a new-technology (with 3-D integration) platform.

The proposed co-design VHDL model is depicted in Fig. 2, while it consists of the following steps: profiling, behavioral optimization, partitioning, kernels mapping into FPGA, kernels mapping into CPU, system integration and back-end tools and configuration and run-time execution.

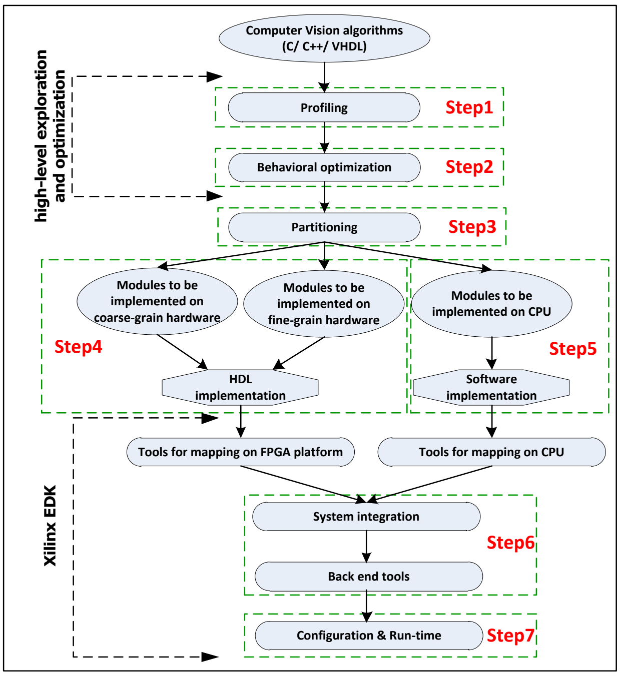

Fig. 2. The employed co-design methodology.

The derived solution with our employed methodology provides a number of trade-offs that balance design criteria among the FPGA device, the employed computer vision algorithms, as well as the entire SPARTAN system. More specifically, these trades-off parameters are summarized as follows: complexity reduction, performance improvement, memory management, parallelism and pipeline extraction

The input to our methodology is a high-level description of SPARTAN's architecture in C/C++, as well as VHDL format. Since the goal of this project is to provide efficient computer vision algorithms with increased performance, our methodology identifies those functionalities that that introduce performance bottleneck in systems' execution and handled appropriately through source-to-source modifications [1]. These modifications will take into account inherent constraints/features taken by the target platform.

The HDL descriptions of the target systems' modules will be mapped on reconfigurable hardware blocks of appropriate type using systematic approaches, mapping tools and reconfigurable hardware generators that are commercially available (Xilinx EDK Framework). The flow is completed with the system integration and back end design phases.

During system integration two different evaluation procedures will take place. Initially, each of the developed computer vision algorithms will be validated in order to verify its proper functionality in respect to timing, performance, and throughput constraints posed by the specifications of SPARTAN project. Possible violations to these constraints will be alleviated by applying focused optimization techniques (e.g. through usage of pipeline/parallelization techniques). Then, we can guarantee that all the developed algorithms meet systems' specifications. Then, one more evaluation step takes place, where the entire system is evaluated against to the same criteria (proper functionality in respect to timing, performance, and throughput constraints). Potential violations in this task will be overcome through appropriately tuning of kernels where validations are identified.

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CONCLUSION

This paper discusses the computer vision algorithms that will be implemented during the SPARTAN project. The implementation medium for these algorithms is a Virtex-6 FPGA device.

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